AMENDMENT

In the claims:

Please replace claims 26, 27, 29, 31, and 33 with the following amended versions of these claims.

26. (Twice Amended) An integrated circuit SRAM cell formed in a semiconductor substrate, a plurality of active transistor regions being formed in the substrate, the SRAM cell comprising:

a first conductive layer disposed on the semiconductor substrate, the first conductive layer forming a plurality of respective control nodes for respective transistors in the substrate;

a second conductive layer disposed over the first conductive layer, the second conductive layer being coupled to the first conductive layer and to active transistor regions to interconnect groups of transistors and thereby form respective data latches;

a plurality of separately planarized spin-on glass layers disposed on the second conductive layer;

an insulating layer disposed on a top one of the planarizing spin-on glass layers; and

a third conductive layer formed on the insulating layer, the third conductive layer being coupled to the data latches to form respective resistive loads for the respective latches.

27. (Twice Amended) The integrated circuit SRAM cell of claim 26 wherein the plurality of separately planarized spin-on glass layers includes a first spin-on glass layer disposed on the second conductive layer, an oxide layer disposed on the first spin-on glass layer, and a second spin-on glass layer disposed on the oxide layer.

29. (Amended) The integrated circuit SRAM cell of claim 26 wherein the first conductive layer comprises a first polysilicon layer and a cladding layer formed on the first polysilicon layer.

31. (Amended) The integrated circuit SRAM cell of claim 26 wherein the second conductive layer comprises a second polysilicon layer and a cladding layer formed on the second polysilicon layer.

33. (Amended) An integrated circuit SRAM cell formed in a semiconductor substrate, a plurality of active transistor regions being formed in the substrate, the SRAM cell comprising:

a first conductive layer disposed on the semiconductor substrate, the first conductive layer forming a plurality of respective control nodes for respective transistors in the substrate;

a second conductive layer disposed over the first conductive layer, the second conductive layer being coupled to the first conductive layer and to active transistor regions to interconnect groups of transistors and thereby form respective data latches;

a plurality of planarizing spin-on glass layers disposed on the second conductive layer;

an undoped oxide layer disposed on a top one of the planarizing spin-on glass layers; and

a third conductive layer formed on the insulating layer, the third conductive layer being coupled to the data latches to form respective resistive loads for the respective latches.

REMARKS

Claims 1 – 34 are pending. Claims 1 – 25 are allowed, and the Applicants have amended claims 26, 27, 29, 31, and 33. As discussed below, claims 26-34 are now in condition for allowance.

The Assignee will surrender the original patent, or submit a declaration as to the loss or inaccessibility of the original patent, after the Examiner allows all of the claims.